

Amendments to the Claims

The listing of claims below replaces all previous versions.

1. (Currently Amended) A method for compressing output data ~~is characterized to~~ comprising:

~~write~~ writing a first data ~~of having a certain first number of bits~~ bit in a corresponding an address of a core cell ~~regions,~~ region;

~~read~~ reading the first data of ~~a certain bit~~ the first number of bits written in the address as read data having the first number of bits;[[,]]

~~compare~~ comparing the ~~written first~~ data and the read data by dividing it ~~to~~ each of the first data and the read data into an upper ~~certain bit~~ portion having a second number of bits and a lower ~~certain bit,~~ portion having a remaining number of bits; and

~~generate~~ generating a 1-bit compressed data ~~of 1-bit~~ for each of the upper portion and the lower portion with ~~an~~ information indicating about whether a ~~fail~~ failure is present.

2. (Currently Amended) A method for compressing output data comprising:

~~a step for~~ reading a first data from a core cell region and prefetching ~~it to a~~ the first ~~certain bit~~ data having a first number of bits in a normal mode;

~~a step for~~ writing the first data of ~~certain bit~~ the first number of bits in a corresponding an address of the core cell region in a test mode;

~~a step for~~ reading the first data of ~~certain bit~~ written in the address of the core cell region and prefetching it the read data;

~~a step for~~ comparing the written first data ~~of certain bit~~ and the read data ~~of certain bit~~ by dividing ~~them to data of~~ each of the first data and the read data into an upper portion having a second number of bits ~~certain bit~~ and ~~data of~~ a lower ~~certain bit~~ portion having a remaining number of bits; and

~~a step for compressing a first error signal of certain of bit result from the comparing to 1-bit generate a compressed data with an information about indicating whether a fail failure is according to a comparing result and generating it present;~~

~~a step for selecting a selected data from the prefetched first data of certain bit prefetched in a normal mode or and the first error signal of certain bit compressed data in a test mode according to a control signal;~~

~~a step for shifting the selected data of certain bit in at an ascending edge and a descending edge of a clock signal and outputting them the selected data serially via one or more a number of output pads in a normal mode;~~

~~a step for shifting the selected data of certain bit in at an ascending edge and a descending edge of the clock signal and outputting them the selected data serially via corresponding one of a number of the one or more output pads in a test mode.~~

3. (Currently Amended) The method for compressing output data as claimed in ~~elame~~ claim 2, wherein

~~the first number of bits associated with the prefetched data, of certain bit or the written first data, and the read data are is 8 bits data;~~

~~the second number of bits associated with the upper portion is 4;~~

~~the remaining number of bits associated with the 8 bits data are divided to upper 4 bits data or lower portion is 4; and~~

~~the compressed data is a 1-bit signal bits data and compressed to 1 bit data with a fail information when it is a test mode.~~

4. (Currently Amended) A packet command driving type memory device comprising:

~~a read data comparing part capable of for receiving a first data and a read data from a core cell region, both the first data and the read data having a first number of bits, and comparing the first data of certain bit read from a core cell region with the read data, and generating a compressed 2-bits data having a second number of bits;~~

~~a data input, output input/output part for shifting capable of transforming the compressed data compressed via the read data comparing part or and the read data read from the core cell region to produce more than one data parts according to a clock signal;~~

an interface part capable of serially ~~for~~ outputting the data parts read from the data ~~input, output input/output~~ part according to the clock signal ~~serially~~ in a packet form via an output pad.

5. (Currently Amended) The packet command driving type memory device as ~~elaimed~~ in claim 4, wherein

~~the first prefetched data of certain bit are~~ number of bits associated with the first data and the read data is 8 bits ~~prefetched data;~~

~~the first data and the read data are divided into, during said comparing, 8 bits of data are divided into an upper 4-bits data or 4-bit portion and a lower 4-bits data 4-bit portion data;~~

~~the second number of bits associated with the compressed data is 2 bits, the read data comparing part compressing the upper or 4-bit portions of the first data and the read data into a first 1-bit signal of the compressed data and the lower 4-bits 4-bit portions of the first data and the read data into a second 1-bit signal of the compressed data are compressed to 1 bit signal; and~~

the data parts include an even-bit data part and an odd-bit data part.

6. (Currently Amended) The packet command driving type memory device as ~~elaimed~~ in claim 4, wherein the read data comparing part comprises:

~~a number plurality of comparators, each of which capable of for receiving and comparing corresponding portions upper or lower 4-bits data of the first data and the read data prefetched 8-bits data according to a control signal and generating 1 bit to generate a 1-bit compressed data with a fail information respectively indicating whether a failure is present; and~~

~~a selecting means capable of for selecting the read data prefetched 8-bits data in a normal mode[[,]] and the compressed 8-bits data generated by one of the plurality of comparators from a corresponding fourth comparator of the numbers of comparators in a test mode according to the control signal.~~

7. (Currently Amended) The packet command driving type memory device as ~~elaimed~~ in claim 6, wherein each of the respective comparator plurality of comparators comprises:

a first ~~to a fourth~~ comparing means capable of ~~for receiving the written 4-bits~~
a first bit of a 4-bit portion of the first data and a first bit of a 4-bit portion of the read
4-bits data and comparing the received two first bits to generate a first 1-bit
comparing signal;

a second comparing means capable of receiving a second bit of the 4-bit
 portion of the first data and a second bit of the 4-bit portion of the read data and
comparing the received two second bits to generate a second 1-bit comparing signal

a third comparing means capable of receiving a third bit of the 4-bit portion of
 the first data and a third bit of the 4-bit portion of the read data and comparing the
received two third bits to generate a third 1-bit comparing signal;

a fourth comparing means capable of receiving a fourth bit of the 4-bit portion
 of the first data and a fourth bit of the 4-bit portion of the read data and comparing the
received two fourth bits to generate a fourth 1-bit comparing signal ~~and comparing~~
~~them by 1 bit and generating a first to a fourth comparing signal according to the~~
~~control signal; and~~

a generating means capable of ~~for~~ receiving the first, the second, the third,
~~and the~~ ~~to a fourth comparing signals~~ signal generated from the first to a fourth
comparing means and generating producing the 1-bit 1-bit compressed data with an
~~information about whether a fail is.~~

8. (Currently Amended) The packet command driving type memory
 device as ~~elaimed~~ in claim 7, wherein each of the first, the second, the third, and to
 the fourth comparing means comprises:

a first NAND GATE ~~for~~ capable of receiving ~~corresponding 1-bit~~ a 1-bit
 signal of the ~~written 4-bits~~ first data and the control signal respectively;

a second NAND GATE ~~for~~ capable of receiving a corresponding 1-bit 1-bit
 signal of the read ~~4-bits data and the control signal;~~

a third NAND GATE ~~for~~ capable of receiving outputs of the first and the
 second NAND GATE;

a first and a second NMOS ~~Transistor~~ transistor having gates and drains
 receiving the outputs of the first and the second NAND GATE;

a first and a second PMOS ~~Transistor~~ transistor connected in series between a
 power voltage and a source of the first and the second NMOS ~~Transistor~~ transistors,
 having gates ~~receiving~~ receive the outputs of the first and the second NAND GATE;

a third PMOS ~~Transistor~~ transistor having a gate ~~receiving~~ receive an output of the third NAND GATE and a source ~~receiving~~ receive a power voltage and drains connected between sources of the first and the second NMOS ~~Transistor~~ transistors and drains of the first and the second PMOS ~~Transistor~~ transistor; wherein
generates the first, the second, the third, and to the fourth comparing signal signals are generated respectively via sources of the first and the second NMOS ~~Transistor~~ transistors ~~connected commonly~~ and drains of the first to the third PMOS ~~Transistor~~ transistors.

9. (Currently Amended) The packet command driving type memory device as ~~claimed~~ in claim 7, wherein the generating means comprises a fourth NAND GATE ~~for~~ receiving the first, the second, the third, and to the fourth comparing signal generated from the first to the fourth comparing means signals as input and generating ~~1-bit~~ the 1-bit compressed data ~~with a fail information~~ as output.

10. (Currently Amended) A packet command driving type memory device comprising:

a ~~number~~ plurality of comparators for receiving and comparing ~~8-bits~~ 8-bit data read from the a core cell region and generating ~~4-bits~~ compressed data, wherein each of the comparators is capable of

receiving and comparing 4 bits of an 8-bit first data and 4 bits of an 8-bit prefetched data read from an address of the core cell region where the first data is written, the received 4 bits of the first data being one of a 4-bit upper portion and a 4-bit lower portion of the first data and the received 4 bits of the prefetched data being one of a 4-bit upper portion and a 4-bit lower portion of the prefetched data,

comparing the 4 bits of the first data and the 4 bits of the prefetched data upper or lower 4 bits data of 8-bits prefetched data in a test mode according to the control signal, and

generating a 1-bit 1-bit compressed data based on a result of the comparing with a fail information respectively indicating whether a failure is present; and

a selecting means ~~for~~ capable of selecting the ~~8-bits~~ 8-bit prefetched data in a normal mode~~[[,]]~~ and the compressed ~~8-bits~~ data from the a corresponding fourth

~~comparator of the numbers of plurality of comparators in the test mode according to the control signal.~~

11. (Currently Amended) A packet command driving type memory device comprising:

a read data comparing part having a ~~number~~ plurality of comparators capable of for

receiving and comparing or an 8-bit first data and an 8-bit prefetched data read from an address of a core cell region where the first data is written,

comparing the received first data with the prefetched data by comparing, via each of the plurality of comparators, corresponding upper or and lower 4 bits data of 8-bits the 8-bit first data and the 8-bit prefetched data according to the control signal in a test mode, and

generating, by each of the plurality of comparators, a 1-bit 2-bits comparing signal compressed data for each of the comparing performed based on corresponding 4 bits portions of the first data and the prefetched data,

a selecting means for selecting a selected data from the 8-bits 8-bit prefetched data in a normal mode[,], and the compressed 8-bits data from the plurality of from a corresponding fourth comparator of the numbers of comparators in a test mode according to the control signal;

a data input, output input/output part for shifting capable of transforming the selected data compressed via the read data comparing part of the data read from the core cell region and transforming it to series into more than one data parts according to a clock signal; and

an interface part for capable of serially outputting the data read parts of the selected data from the data input, output input/output part according to the clock signal serially via an output pad.